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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,594	10/31/2001	David J.C. Johnson	10013444 -1	1931

7590 02/25/2004

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EXAMINER	
CHACE, CHRISTIAN	

ART UNIT	PAPER NUMBER
2187	3

DATE MAILED: 02/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/001,594	Applicant(s) JOHNSON ET AL.	
	Examiner Christian P. Chace	Art Unit 2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

IDS submitted 20 February 2002, has been considered by examiner and entered as paper number two. A signed and initialed copy is attached hereto.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Cheng et al (US Patent 5,655,103).

With respect to independent claim 1, a cache memory system is disclosed in figure 1, #101, for example, which shows a CPU and cache.

Storage for a plurality of data values is disclosed in figure 3 as an address, inclusion, and cross-interrogation bits, which are, of course, "data values." In addition, a cache, as shown in figure 1 #101, is a storage for a plurality of data vaues.

Storage for a plurality of "age bits," each age bit corresponding to one of the data values is disclosed in figure 3 as the "stale bit."

Each age bit indicating whether the corresponding data value is stale is disclosed in figure 3 as the "stale bit." The stale bit is also discussed in the abstract, for example.

With respect to claim 2, each age bit indicating that the corresponding data value is stale is, again, disclosed in figure 3 and the abstract, as discussed supra.

Indicating that the age bit is stale when the age bit has remained at a particular logical state (stale bit set to zero) of at least a "predetermined time period," is disclosed in the abstract as "[i]f the processor further modifies the cache line." In other words, the time it takes the processor to further modify the cache line is the "predetermined time period."

With respect to claims 3 and 6, a state machine is disclosed in column 2, lines 31-32 as the memory controller.

The state machine "periodically" (see discussion of "predetermined time period" supra with respect to claim 2) determining the state of each age bit is discussed in the abstract as "setting the age bit."

For each age bit that is not at the particular logical state, setting the age bit to the particular logical state is disclosed in the abstract, as discussed supra with respect to claim 1, and is also disclosed in column 2, lines 31-32 as "setting the stale bit."

With respect to claim 4, each age bit further indicating whether the corresponding data value is modified is disclosed in the abstract as, "If the first processor further modifies the cache line...the stale bit is set to one." In other words, the stale bit set to one indicates the data is modified, as well as stale.

With respect to claim 5, each age bit indicating that the corresponding data value is stale and modified is disclosed in the abstract as, "If the first processor further modifies the cache line...the stale bit is set to one." In other words, the stale bit set to one indicates the data is modified, as well as stale.

Doing so when the age bit has remained at a particular logical state for at least a predetermined time period is disclosed in the abstract as "[i]f the processor further modifies the cache line." In other words, the time it takes the processor to further modify the cache line is the "predetermined time period."

With respect to independent claim 7, a method of indicating whether an entry in a cache memory is stale is disclosed in the abstract.

Setting a bit to a first logical state when the entry is "accessed," is disclosed in the abstract as setting the stale bit equal to zero. "Accessing" is a load/miss request from a processor. Column 1, lines 17-21 and lines 27-28 discuss load/miss supplying (accessing) data to the CPU/[cache] (shown as one unit in figure 1, #101, for example.)

Setting the bit to a second logical state is disclosed in the abstract as setting the stale bit to one.

Determining that the entry is stale when the bit is at the second logical state after at least a "predetermined time" after being set to the second logical state is disclosed in the abstract as "[i]f the processor further modifies the cache line." In other words, the time it takes the processor to further modify the cache line (thereby setting the stale bit to the second logical state, or one) is the "predetermined time period."

With respect to independent claim 8, a method of detecting whether an entry in a cache memory is stale and dirty is disclosed in the abstract.

Setting a bit to a first logical state when the entry is "written," is disclosed in the abstract as setting the stale bit equal to zero. "Writing" is a load/miss request from a

processor. Column 1, lines 17-21 and lines 27-28 discuss load/miss supplying (writing) data to the CPU/[cache] (shown as one unit in figure 1, #101, for example.)

Setting the bit to a second logical state is disclosed in the abstract as setting the stale bit to one.

Determining that the entry is stale and dirty (modified) when the bit is at the second logical state after at least a "predetermined time" after being set to the second logical state is disclosed in the abstract as "[i]f the processor further modifies the cache line." In other words, the time it takes the processor to further modify the cache line (thereby setting the stale bit to the second logical state, or one) is the "predetermined time period."

"If the first processor further modifies the cache line...the stale bit is set to one." In other words, the stale bit set to one indicates the data is modified, as well as stale.

With respect to independent claim 9, a method of detecting whether at least one entry in a set of entries in a cache memory is stale is disclosed in the abstract.

Setting a bit to a first logical state when the entry corresponding to an index is "accessed," is disclosed in the abstract as setting the stale bit equal to zero. The "index" is the dependency table shown in figure 3. As discussed with respect to independent claim 1, the index holds a "stale bit" value, which is the instantly claimed "bit." "Accessing" is a load/miss request from a processor. Column 1, lines 17-21 and lines 27-28 discuss load/miss supplying (accessing) data to the CPU/[cache] (shown as one unit in figure 1, #101, for example.)

Setting the bit to a second logical state is disclosed in the abstract as setting the stale bit to one.

Determining that at least one entry in the corresponding index is stale when the bit is at the second logical state after at least a "predetermined time" after being set to the second logical state is disclosed in the abstract as "[i]f the processor further modifies the cache line." In other words, the time it takes the processor to further modify the cache line (thereby setting the stale bit to the second logical state, or one) is the "predetermined time period."

With respect to independent claim 10, a method of detecting whether at least one entry in a cache memory is stale and dirty is disclosed in the abstract.

Setting a bit to a first logical state when an entry "corresponding to an index" is modified is disclosed in the abstract as setting the stale bit equal to zero. The "index" is the dependency table shown in figure 3. As discussed with respect to independent claim 1, the index holds a "stale bit" value, which is the instantly claimed "bit."

Setting the bit to a second logical state is disclosed in the abstract as setting the stale bit to one.

Determining that the entry is stale and dirty (modified) when the bit is at the second logical state after at least a "predetermined time" after being set to the second logical state is disclosed in the abstract as "[i]f the processor further modifies the cache line." In other words, the time it takes the processor to further modify the cache line (thereby setting the stale bit to the second logical state, or one) is the "predetermined time period."

"If the first processor further modifies the cache line...the stale bit is set to one." In other words, the stale bit set to one indicates the data is modified (dirty), as well as stale.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian P. Chace whose telephone number is 703.306.5903. The examiner can normally be reached on 9-4-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703.308.1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christian P. Chace